

## **Phase Multiplier Circuit**

### **RELATED APPLICATION**

This application claims the benefit of priority pursuant to 35 USC §119(e) from U.S. provisional patent application Ser. No. 60/445,657, filed February 7, 2003, and entirely incorporated herein by reference.

### **BACKGROUND OF THE INVENTION**

The function of a phase multiplier circuit is to generate equal-frequency output signals, each having a phase, from an input signal. In one embodiment, the phases of the output signals are evenly spaced between 0 and 360 degrees.

Fig. 1 is a schematic diagram illustrating an example of a phase multiplier of the prior art. This circuit is commonly referred to as a delay-locked loop. A voltage-controlled delay line 2 is coupled to an input signal IN and is comprised of five voltage-controlled delay subcircuits U1, U2, U3, U4, and U5, and has four outputs: OUT1, OUT2, OUT3, and OUT4.

Also included in Fig. 1 is a phase detector 3, a charge pump 4, a loop filter capacitor C1, a reset transistor M3, a reset inverter U12, and a reset synchronization flip-flop U10. The phase detector includes flip-flops U6 and U7, AND gate U8, and OR gate U9. The charge pump includes transistors M1 and M2, and inverter U11. The voltage of a CONTROL node controls the delay through the delay subcircuits. Coupled to the CONTROL node is the charge pump, the loop filter capacitor, and the voltage controlled delay line.

Initially, the delay-locked loop is reset by asserting RESET high. In this state, the voltage of the CONTROL node is set to AVDD, forcing the delay through the delay line to a minimum, and the phase detector is also reset. Through action of U10, phase detector reset signal RESETX is

synchronous to the rising edge of IN. Subsequent to the falling edge of RESET, RESETX must fall immediately after the rising edge of IN but before the rising edge of FB. D flip-flop U10 ensures that this occurs by synchronizing RESETX to the rising edge of IN.

After RESET is deasserted low, and by adjusting the voltage of the CONTROL node in a negative feedback loop, the delay-locked loop increases the delay of the delay line until the phase of FB is equal to the phase of OUT1. It then follows that the phases of the output signals are equally spaced about 360 degrees, but only if the delay subcircuits are well matched, and the phase error between FB and OUT1 is zero. These two requirements to achieve equal spacing can be difficult to meet. By eliminating the phase detector and by measuring and adjusting the delays of delay subcircuits individually, the present invention effectively eliminates these requirements for equal phase spacing.

## SUMMARY OF THE INVENTION

So as to generate multiple output signals whose phases are evenly spaced about 360 degrees, and having a frequency equal to that of an input signal, a phase multiplier circuit includes three or more instances of a phase multiplier subcircuit and additional circuitry configured in a negative feedback loop.

The particular utility and value in this phase multiplier circuit is the use of circuitry to measure, and feedback to control, the phases of the output signals such that they are accurately and evenly spaced between 0 and 360 degrees. Small (and, therefore, low-power but poorly-matched) transistors are used to generate a delay from each output signal to the next, and relatively large (and, therefore, well-matched) transistors operating at low power are used to

measure the relative phases of the generated signals. This approach simultaneously achieves the desirable goals of both accurate phase control and low power.

### BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a schematic diagram of a phase multiplier circuit of the prior art.

Fig. 2 is a schematic diagram of the phase multiplier subcircuit, in accordance with the present invention.

Fig. 3 is a schematic diagram of the phase multiplier circuit, in accordance with the present invention.

Fig. 4 illustrates phase multiplier circuit waveforms.

Fig. 5 illustrates the output signals of the phase multiplier circuit.

Fig. 6 is a schematic of a buffer.

Fig. 7 is a schematic of a buffer.

Fig. 8 is a schematic of dual-gate transistors and particular implementations thereof.

### DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Three instances of the phase multiplier subcircuit of Fig. 2 and additional circuitry comprise the phase multiplier circuit of Fig. 3. The phase multiplier subcircuit of Fig. 2 comprises a difference circuit 11, a loop filter transistor M10, a reset transistor M11, a BIASN generation circuit 14, a voltage controlled delayed circuit 15, and a buffer 16.

The difference circuit 11 converts a phase delay to a phase current and subtracts this phase current from a bias current. Difference circuit 11 comprises p-channel dual-gate transistor XDG1 having a source coupled to common node COMMON, and first and second gate inputs coupled

to inputs /INB and OUTB; a first current mirror comprising n-channel transistors **M1** and **M2**, and bias current source transistor **M3**. Transistor **XDG1** sources a first current during a period of time when inputs /INB and OUTB are both low, and this period of time is a measure of a phase delay from a falling edge of /INB to a rising edge of OUTB. The first current is mirrored by the current mirror which has an output which sinks the phase current. The phase current and the bias current are respectively conducted through the output of the current mirror and the drain of transistor **M3**, and this output and drain are coupled to the BIASP integration node. Also coupled to BIASP is the loop filter transistor **M10**; reset transistor **M11**; and current mirror **14**, comprising p-channel transistor **M4** having a drain coupled to bias node BIASN and a gate coupled to BIASP, and n-channel transistor **M5** having a gate and drain coupled to BIASN. The gate of transistor **M3** is coupled to input PULLUPBIAS.

Coupled to the BIASP integration node and the BIASN bias node is the voltage controlled delay circuit **15**, comprising dual-gate n-channel transistors **XDG3** and **XDG5**, and dual-gate p-channel transistors **XDG2** and **XDG4**. First gate inputs of **XDG2** and **XDG3** are coupled to input signal INA, second gate inputs of **XDG2** and **XDG4** are coupled to BIASP, and second gate inputs of **XDG3** and **XDG5** are coupled to BIASN. Drains of **XDG2** and **XDG3** are coupled together and to first gate inputs of **XDG4** and **XDG5**. Drains of **XDG4** and **XDG5** are coupled together and to output OUTA and to the input of inverter **U1**. The output of **U1** is coupled to output /OUTB and to the input of inverter **U2**. The output of **U2** is coupled to output OUTB.

Fig. **3** illustrates the phase multiplier circuit, comprising an interconnection of multiple instances of the phase multiplier subcircuit and additional circuitry. The phase multiplier circuit further comprises a current source **I1**, a circuit **21** for converting a second measure of phase

delay to a bias voltage  $V_{\text{PULLUPBIAS}}$ , three interconnected phase multiplier subcircuits **22**, and a buffer **23**.

Current source **I1** is coupled between power supply AVDD and common node COMMON.

Circuit **21** of the phase multiplier circuit converts a phase delay to the bias voltage  $V_{\text{PULLUPBIAS}}$  and comprises p-channel dual-gate transistor **XDG6** having a source coupled to common node COMMON, and first and second gate inputs coupled to inputs /OUTB4 and OUTB1; a second current mirror comprising n-channel transistors **M6** and **M7**; and diode-connected p-channel transistor **M8**. Transistor **XDG6** sources a second current during a period of time when inputs /OUTB4 and OUTB1 are both low. This period is the second measure of phase delay, and is equal to the time from a falling edge of /OUTB4 to a rising edge of OUTB1. The second current is mirrored by the second current mirror which has an output coupled to PULLUPBIAS and to the gate and drain of transistor **M8**. Transistor **M3** of each phase multiplier subcircuit of Fig. 2 and transistor **M8** form current mirrors having a gain substantially equal to one.

The first current mirror of difference circuit **11** and the second current mirror of circuit **21** are matched to each other, and in a preferred embodiment, the current gain of each of these current mirrors is substantially less than one.

The three interconnected phase multiplier subcircuits **22** comprise first, second, and third phase multiplier subcircuits **U3**, **U4**, and **U5**. The first phase multiplier subcircuit has first and second inputs INA and /INB coupled to IN and /OUTB1, and first, second, and third outputs OUTA, /OUTB, and OUTB coupled to OUTA2, /OUTB2, and OUTB2. The second phase multiplier subcircuit has first and second inputs INA and /INB coupled to OUTA2 and /OUTB2,

and first, second, and third outputs OUTA, /OUTB, and OUTB coupled to OUTA3, /OUTB3, and OUTB3. The third phase multiplier subcircuit has first and second inputs INA and /INB coupled to OUTA3 and /OUTB3, and first, second, and third outputs OUTA, /OUTB, and OUTB coupled to OUTA4, /OUTB4, and OUTB4.

Buffer 23 comprises first and second inverters. The first inverter U1 has an input coupled to IN and an output coupled to /OUTB1, and the second inverter U2 has an input coupled to /OUTB1 and an output coupled to OUTB1.

In a preferred embodiment, outputs OUTBn ( $n=1,2,3,4$ ) comprise the output signals. Using circuit 21 and each transistor M3 of the phase multiplier subcircuits, a bias current is generated within each of the phase multiplier subcircuits which is substantially in proportion to the second measure of a phase delay. Also within each phase multiplier subcircuit the difference circuit subtracts the bias current from the phase current. A stable, steady-state operating point of the phase multiplier circuit occurs when for each phase multiplier subcircuit, the bias current is equal to the phase current. By extension, the second measure of phase delay and each measure of the phase delay of the phase multiplier subcircuits will also be equal. Further, this ensures that the phase of each of the output signals OUTBn ( $n=1,2,3,4$ ) will be substantially equally spaced about 360 degrees, as desired.

Fig. 4 illustrates sample waveforms of input RESET and outputs BIASPn ( $n=1,2,3$ ) of the phase multiplier subcircuits. The voltages of outputs BIASPn ( $n=1,2,3$ ) transition from an initial state to a final state following the de-assertion of RESET from a logic high level to a logic low level.

Fig. 5 illustrates sample waveforms of the output signals OUTB<sub>n</sub> (n=1,2,3,4) after the BIASP nodes of the phase multiplier subcircuits have transitioned to their final values. In steady state, each phase current is equal to a bias current, and the phases of OUTB<sub>n</sub> (n=1,2,3,4) 40, 41, 42, and 43 are substantially equal to 90°, 180, 270, and 360 degrees. This is the desired result.

Fig. 6 illustrates logic inverters U1 and U2 of buffer 15 of the phase multiplier subcircuit of Fig. 2, and Fig. 7 illustrates logic inverters U3 and U4 of buffer 23 of the phase multiplier circuit of Fig. 3.

Fig. 8a illustrates two possible circuit choices for dual-gate transistor XDG2 of Fig. 2, and Fig. 8b illustrates two possible circuit choices for dual-gate transistor XDG3 of Fig. 2. Similar circuit choices exist for dual-gate transistors XDG1, XDG4, and XDG5 of Fig. 2, and XDG6 of Fig. 3.

In Figs. 2, 3, 6, and 7, the following nodes are coupled together with other nodes of the same name: COMMON, PULLUPBIAS, AVSS, and AVDD.

The following claims describe the generation of four output signals using three interconnected phase multiplier subcircuits and additional circuitry. Those skilled in the art will recognize that through the use more than three phase multiplier subcircuits, more than four output signals can be generated. Except to the extent specified in the following claims, the circuit configurations and device sizes shown herein are provided as examples only. Those skilled in the art will recognize that desired and proper circuit operation can be achieved with many other circuit configurations, device sizes, and/or combinations of device sizes.

The phase multiplier circuit can be implemented with discrete components, with semiconductor devices embedded in an integrated circuit such as an application specific

integrated circuit (ASIC), or with a combination of both. Individual signals or devices can be active high or low, and corresponding circuitry can be converted or complemented to suit any particular convention. The term "coupled" used in the claims includes various types of connections or couplings and includes a direct connection or a connection through one or more intermediate components.